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A design of FPGA based intelligent data handling interfacing card.

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Abstract
With the increasing demand in the custom built logic for avionics systems, FPGA is used in this proposed interfacing card design. This FPGA based intelligent data handling card (IDHC) for the IVHM system, will interface the data from aircraft subsystems to the aircraft digital data bus. This IDHC interfacing card is based on the Virtex-5 FPGA (Field Programmable Gate Array), which provides flexibility by re-programming, so that it can be configured to the required functionality. Fault detection can be done within the FPGA and only the anomalies passed to the computer, so that the bus bandwidth can be utilized effectively and also excessive wiring can be eliminated, that would have been required for multiple individual systems. The work concentrates on designing the schematic using OrCAD.
Keywords: DCU, FPGA, IDHC, Intelligent, IVHM, Reconfiguration.

I. Introduction

Integrated Vehicle Health Management system (IVHM) is a system which enables automatic detection, diagnosis, prognosis and mitigation of adverse events arising from components failures [1]. Aircraft health monitoring system as a concept has challenges to enhance flight safety and at the same time to reduce operational and maintenance costs [2]. The IVHM helps in improving the overall safety of an aircraft and also reducing both maintenance and operational costs. So IVHM is increasingly being adopted in various aircraft programs.

An Integrated Vehicle Health Monitoring system is to improve the vehicle safety, reduce maintenance costs, and improve vehicle readiness by identifying potential faults and failures, taking the proper corrective actions, and updating to the responsible crew member about the vehicle health and condition [3]. This is done by capturing data by a network of sensors and analyzing the data using life prediction algorithms implemented on highly evolved software systems.

In the IVHM system, the Data Concentrator Units (DCUs) collect discrete inputs, analog signals, and digital data from sensors and equipment throughout the aircraft, then convert them to digital format for streaming over the databus of the flight-control or aircraft-management system [4]. Most of the DCUs available are processor based units.

The demand for custom logic within today's avionics industry has led to the increase of Field Programmable Gate Arrays (FPGAs) in aircraft electronic systems. This demand, along with technological advances in size and speed, are resulting in the integration of multiple electronic functions into one chip. To accomplish this, designers are starting to look to FPGA designs. The FPGA provides dynamically reconfigurable capabilities & thus it has revolutionized the digital systems [5].

This paper describes the design of an FPGA based interfacing card for IVHM system.

II. Description

The objective of this work is to design an intelligent data handling card (IDHC) for the IVHM system. The IDHC is an interfacing card, which will interface the data from different aircraft subsystems to the aircraft digital data bus, in the IVHM system. The paper concentrates on designing the schematic and checking the Design rule check (DRC) & Netlist is done for error free design.

This device will consist of a programmable and interfacing device. It collects the inputs in the form of discrete or analog signals, or digital data, which are from different subsystems and equipment of the aircraft, and does the processing if required & then converts them to digital format for streaming over the digital data bus.

The IDHC will have the functionality like data concentration, sub-system fault diagnosis and the effective utilization of the bus bandwidth by passing only the anomalies. Since it contains a programmable device it is reconfigurable. Main advantages include re-configurability, reduced cabling and minimal signal interference, as well as improved robustness and survivability.

The IVHM system, block diagram is shown in Fig 1, the data from different aircraft subsystems is

passed on to the aircraft digital data bus through the IDHC card & the aircraft digital data bus is interfaced to the main or IVHM computer.

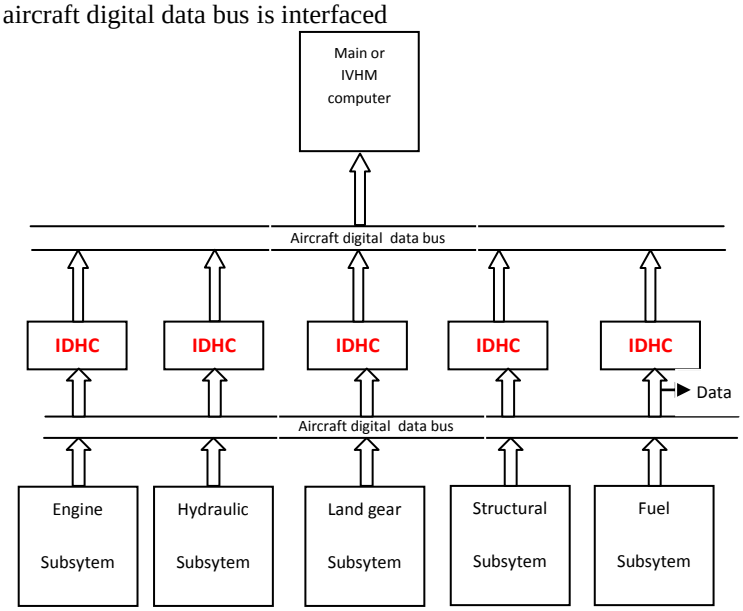

Fig1. Block diagram of IVHM system

III. Block diagram of IDHC

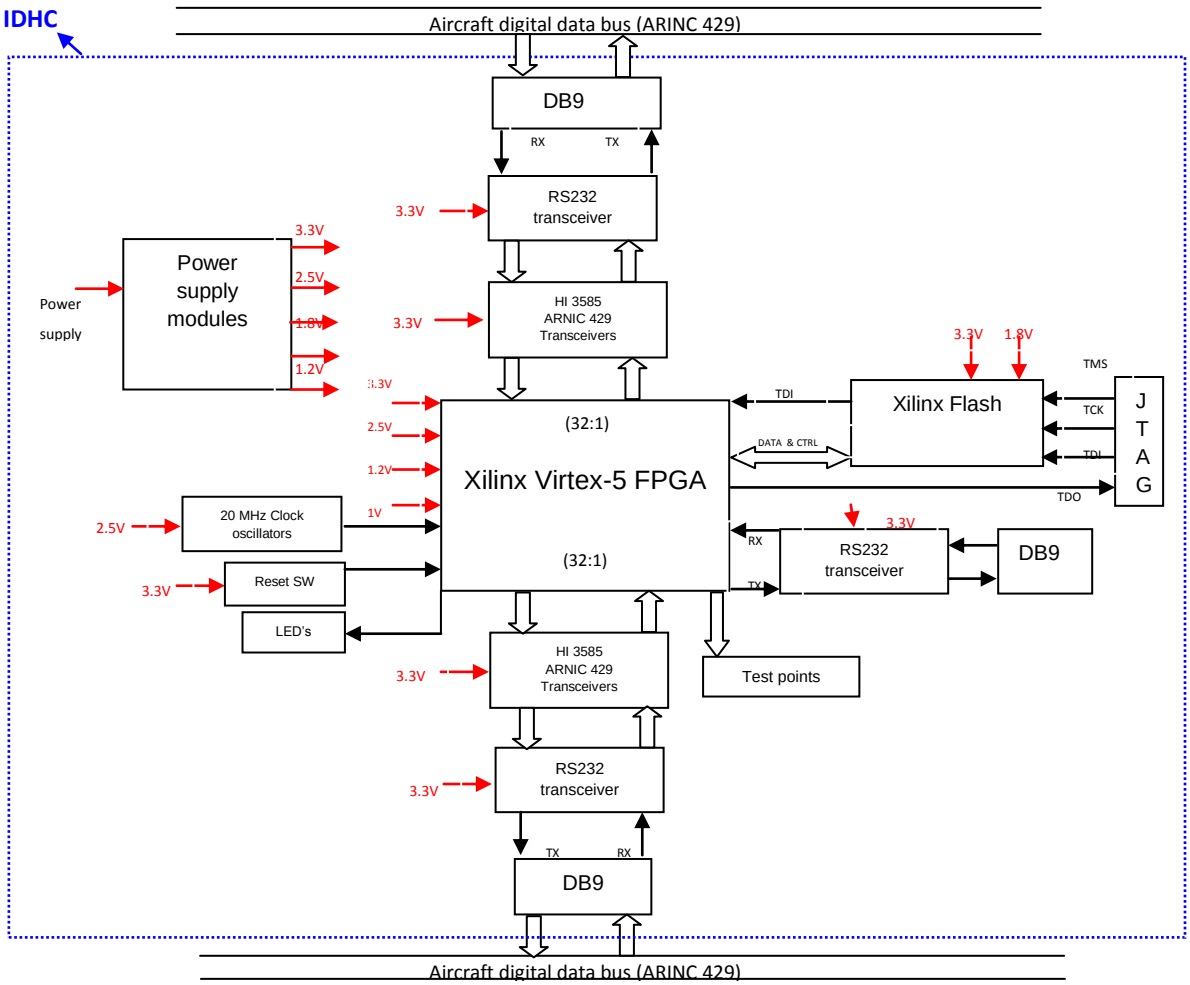

Fig2. Block diagram of IDHC

3.1 Block diagram description

The block diagram of the intelligent data handling card (IDHC) is shown in Fig 2.

The IDHC interfacing card is based on the Virtex-5 FPGA, this card will collect, combine and reformat data from different aircraft subsystems into the required avionics bus format. It is used to control multiple systems and to monitor the health of systems. The block diagram shows that the Input data are received into the FPGA and does the processing if required & converts the data to the required digital data format, and passes it to the Main or IVHM computer through the aircraft digital data bus (ARINC 429).

The card is based on FPGA, Since FPGA is a programmable device it is reconfigurable, so that different functionality can be implemented. The FPGA is a volatile memory so Flash memory is used for storing the FPGA configuration bits. Since FPGA and other devices on the board require different voltages for their operations, the power section is designed to generate different voltages. A 20 MHz crystal oscillator is connected to the FPGA, so that it gets the required clock input. External ARINC 429 transceivers are used for interfacing to the ARINC 429 digital data bus through the DB9 connector. Another RS232 transceiver is interfaced to the FPGA for the debugging purpose. The LEDs are placed on the board to indicate the different status, according to the requirement the particular LED will glow. The test points are connected for debugging purpose.

The schematic design is carried out using OrCAD tool, OrCAD is an EDA (Electronic Design Automation) tool from Cadence used for the designing layout of printed circuit boards (PCBs). Orcad capture is a versatile design entry product used to create the schematic for analog or mixed signal designs, PCB layout designs and PLD. Then the DRC (Design Rule Check) is done, DRC property helps in debugging any design rule violations that might have occurred during the schematic entry process; then the netlist is generated in different formats depending upon the requirements. This netlist is used in the fabrication of the PCB. The netlist generated is compared with the schematic design to make sure the design is error free.

3.2 Component description

FPGA: Virtex-5 devices are user-programmable gate arrays with various configurable elements and embedded cores optimized for high-density and high-performance system designs. The Virtex-5 FPGA will be configured in the Master Serial mode using Xilinx Platform flash PROM. FPGA can also be configured using JTAG connection. Xilinx Platform flash PROM will be programmed using JTAG interface [6].

SPROM: In-System Programmable PROMs for Configuration of Xilinx FPGAs. PROMs provide an easy-to-use, cost-effective, and reprogrammable method for storing large Xilinx FPGA configuration bitstreams [7].

HI-3585: The HI-3585 from Holt Integrated Circuits is a silicon gate CMOS device for interfacing a Serial Peripheral Interface (SPI) enabled microcontroller to the ARINC 429 serial bus. The device provides one receiver with user-programmable label recognition for any combination of 256 possible labels, 32 x 32 Receive FIFO and analog line receiver. The independent transmitter has a 32 x 32 Transmit FIFO and built-in line driver. The HI-3585 applies the ARINC 429 protocol to the receiver and transmitter [8].

ARINC 429: Aeronautical Radio, Incorporated (ARINC) 429 is a two-wire, point-to-point unidirectional data bus that is application-specific for commercial and transport aircraft. The connection wires are twisted pairs. Words are 32 bits in length and most messages consist of a single data word using bipolar RZ format [9].

Power Supply Modules: According to the requirements of the design, different voltages like 1V, 1.2V, 1.8V, 2.5V and 3.3V are generated for different components in the design, by using corresponding voltage regulators.

JTAG: The JTAG connector is for Programming of FPGA and Configuration PROM, the FPGA and its Configuration PROM will be connected in a 3.3V JTAG chain.

RS232 transceiver: RS232 transceiver is provided which is connected to the DB9 Female connector, which is for the debug purpose.

IV. Conclusion

A schematic design as been carried out for an FPGA based interfacing card which will be used in the IVHM system. This card will interface the data from aircraft subsystems to the aircraft digital data bus. Since it is based on FPGA, it provides flexibility by re-programming. The intelligence can be built with in the FPGA and only the anomalies passed to the computer, so that the bus bandwidth can be utilized effectively. Also the excessive wiring that would have been required for multiple individual systems is eliminated.

The components were analysed and chosen according to the design requirements. The libraries for all the required components were created and then the schematic design is done using the OrCAD tool. The Design Rules Check (DRC) is done for

debugging whether any design rule violations have occurred during the schematic process and the net list generated is compared with the schematic design to make sure the design is error free.

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